Amendments to the Claims:

Please amend claims 5 and 8 as indicated below.

Please add new claims 9-12 as presented below.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-4 (canceled)

Claim 5 (currently amended): A data transmission device for serial synchronous data transmission comprising:

a master device including a first arithmetic unit and a master interface; and

a slave device including a second arithmetic unit and a slave interface;

wherein:

the master and slave interfaces are capable of being connected via at least one data transmission line and a clock signal line;

the master and the slave interfaces are capable of being connected via ~~a~~ an acknowledgment signal line configured for a transmission of an acknowledgment signal from the slave device to the master device;

the second arithmetic unit is capable of generating the acknowledgment signal upon completion of a data reading operation; and

the first arithmetic unit is configured so that a capability of the master device to initiate a further write operation to the slave device is dependent upon a receiving of the acknowledgment signal from the slave device.

Claim 6 (previously presented): The data transmission device as recited in claim 5 wherein the at least one data transmission line is a single bidirectional data transmission line.

Claim 7 (previously presented): The data transmission device as recited in claim 5

wherein the at least one data transmission line includes a first and a second unidirectional data transmission line.

Claim 8 (currently amended): A method for serial synchronous data transmission in a data transmission device including a master device and a slave device, the master device including a first arithmetic unit and a master interface, the slave device including a second arithmetic unit and a slave interface, the master and slave interfaces being connected via a first and a second unidirectional data transmission line, an acknowledgment signal line, and a clock signal line, the method comprising:

initiating, using the master device, a communication by transmitting a first transmit bit;

receiving, using the slave device, the first transmit bit after a first master-slave transmission delay;

activating, using the master device, the clock signal after a first clock signal delay time;

receiving, using the slave device, an interrupt signal from the clock signal line after a second master-slave transmission delay;

transmitting, using the slave device, a first receive bit; ~~and~~

reading, using the slave device, the first transmit bit while applying a first interference suppression measure;

receiving, using the master device, the first receive bit after a first slave-master transmission delay;

activating, using the slave device, a first acknowledgment signal after a first delay time;

receiving, using the master device, the first acknowledgment signal after a second slave-master transmission delay;

deactivating, using the master device, the clock signal;

initiating, using the master device, a new cycle by transmitting a second transmit bit;

reading, using the master device, the first receive bit while applying a second interference suppression measure;

receiving, using the slave device, the second transmit bit and a first deactivated clock

signal after a third master-slave transmission delay;

activating, using the master device, the clock signal after a second clock signal delay time;

deactivating, using the master device, the first acknowledgment signal after a third slave-master transmission delay;

receiving, using the slave device, a first active clock signal after a fourth master-slave transmission delay;

transmitting, using the slave device, a second receive bit;

reading, using the slave device, the second transmit bit while applying a third interference suppression measure;

receiving, using the master device, the second receive bit after a fourth slave-master transmission delay;

activating, using the slave device, a second acknowledgment signal after a second delay time;

receiving, using the master device, the second acknowledgment signal after a fifth slave-master transmission delay;

deactivating, using the master device, the clock signal;

transmitting, using the master device, a third transmit bit;

reading, using the master device, the second receive bit while applying a fourth interference suppression measure;

initiating, using the master device, a last cycle by:

transmitting a last transmit bit;

deactivating the clock signal; and

reading a receive bit of a previous cycle while applying a fifth interference suppression measure;

receiving, using the slave device, a last transmit bit and a second deactivated clock signal after a fourth master-slave transmission delay;

activating, using the master device, the clock signal after a third clock signal delay time;

deactivating, using the master device, a third acknowledgment signal after a sixth slave-master transmission delay;

receiving, using the slave device, a second active clock signal after a fifth master-slave transmission delay;

transmitting, using the slave device, a last receive bit;

reading, using the slave device, the last transmit bit while applying a sixth interference suppression measure;

receiving, using the master device, the last receive bit after a seventh slave-master transmission delay;

activating, using the slave device, a fourth acknowledgment signal after a third delay time;

receiving, using the master device, the fourth acknowledgment signal after an eighth slave-master transmission delay;

setting, using the master device, the clock signal to an inactive resting level;

reading, using the master device, the last receive bit while applying a seventh interference suppression measure;

setting, using the slave device, the first unidirectional data transmission line inactive after a sixth master-slave transmission delay;

deactivating, using the master device, the clock signal after the reading the last receive bit;

deactivating, using the slave device, a third active clock signal after a seventh master-slave transmission delay; and

deactivating, using the master device, a fifth acknowledgment signal after a ninth slave-master transmission delay.

Claim 9 (new): The data transmission device as recited in claim 5 wherein the second arithmetic unit is configured to receive data of the data reading operation from the master device and to generate and send to the master device a receive bit as only a single bit after a receiving of the data.

Claim 10 (new): The data transmission device as recited in claim 5 wherein the first arithmetic unit is configured to generate and send data of the data reading operation to the slave device as only a single transmit bit.

Claim 11 (new): The method for serial synchronous data transmission wherein the transmitting the first receive bit is performed by transmitting only a single bit.

Claim 12 (new): The method for serial synchronous data transmission wherein the transmitting the first transmit bit is performed by transmitting only a single bit.